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FPGA Based Facial Recognition System

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Authors' contributions

This work was carried out in collaboration among all authors. Authors MI and MKN designed the study, performed the statistical analysis, wrote the protocol and wrote the first draft of the manuscript. Authors MBA and AUT managed the analyses of the study. Authors MUI, MBA and MG managed the literature searches. All authors read and approved the final manuscript.

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ABSTRACT

Introduction: Face recognition research is motivated not just by fundamental security concerns, but also by the fact that it is required in many practical applications where human identity is required. Rapid improvements in technology such as digital cameras, the internet, mobile devices, and technological demands on security have facilitated and encouraged face recognition as one of the key biometric technologies. Face detection, feature extraction, and classification methods for face identification utilizing hardware description language HDL implemented in a Field Programmable Gate Array are investigated in this paper (FPGA).The research goals include.

Methods: The Viola-Jones algorithm for face detection was developed, followed by developing an algorithm for feature extraction using Artificial Neural Networks (ANN),and finally feature matching using Hamming Distance. The whole system was implemented on FPGA, using VHDL.

Results: The system successfully identifies the eye region of the face from the image, and extracts the features of each image then perform matching. The program output or display a result of image matched or image not matched. The execution time of the overall system speeds up due to the parallel processing of FPGA.

Conclusion: The program was able to distinguish between two images of people based on their eye image, as well as detect minor expressional changes in the test image. Designing the full algorithm using FPGA help in speeding up the execution time of the processes, which gives the opportunity to build the system to work in real time with low cost due to its flexibility.

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Keywords: FPGA; ANN; viola jones algorithm; VHDL; Hamming distance.

1. INTRODUCTION

Biometric recognition is the automatic identification of a person based on one or more physical or behavioral characteristics. A biometric identification system, in general, employs physical characteristics (like a fingerprint, iris pattern, or face) or behavioral patterns (like handwriting, voice, or keystroke pattern) to identify a person. Face recognition has become a significant component of biometric recognition procedures. It is a significant research problem that cuts across many fields and disciplines. Face recognition is a fundamental human trait that is crucial for good communications and interactions among people, in addition to having several practical uses such as bankcard identification, access control, mug shot searches, security monitoring, and surveillance systems.

Instead of considering the entire face, specific sections of the face were excised in this study, which is known as hemi-facial extraction [1]. The eye region was chosen since the eyes can never be hidden, even when wearing various disguises on the face, and so recognition will be simple and accurate. An Artificial Neural Network (ANN) is a type of information processing system made up of a large number of interconnected components called neurons, typically, a neural network system has three or more layers. Neural network properties may be used to imitate some functions of biological brains and neural systems. In this work the back propagation neural network algorithm was adopted Self-organization, adaptive learning, and fault tolerance are the main benefits of neural networks. Neural networks are employed in many biometric recognition challenges because of these properties. The use of a Field Programmable Gate Array (FPGA) for neural network implementation gives programmable systems more flexibility. FPGAs combine great efficiency with adequate flexibility, making them an excellent choice for neural network implementation. Aside from having the right speed for real-time applications, FPGAs can be reprogrammed as many times as needed at no extra expense.

The basic FPGA architecture is a two-dimensional array of logic blocks and flip-flops with ways for the user to set each logic block's function, inputs/outputs, and block interconnection. Design entry in a conventional FPGA design flow begins with schematics or a hardware description language (HDL), such as Verilog HDL or VHDL [2]. A hardware description language (HDL) is a computer language used to describe electronic circuits in a formal way. It can describe a circuit's functioning, structure, and input stimuli in order to check that the operation is correct using simulation. The aim of this study is to design of facial recognition system based FPGA.

2. LITERATURE REVIEW

A back propagation neural network BPNN model for extracting the basic face of human face pictureswas developed [3]. The eigenfaces are then projected onto human faces in order to detect distinct feature vectors. [4] suggested a gray-scale face recognition system. To decrease the complexity of ANN training, they used it in the pattern recognition phase rather than the feature extraction phase. [5] also used a 3D facial recognition system with geometrics approaches and two types of ANN to conduct face recognition (multilayer perceptron and probabilistic). [6] focused on a face recognition approach based on PCA and the BP algorithm. PCA is used to extract the feature, and the BPNN is used to classify it.A low-cost real-time facial recognition architecture based on a Field Programmable Gate Array (FPGA) was reported in [7]. The face recognition module accepts faces from a video stream and processes them using the widely used Eigen faces technique, commonly known as the Principal Component Analysis (PCA) algorithm. [8] suggested a neural network-based handwritten signature categorization method with FPGA implementation. Very High Speed Integrated Circuits Hardware Description Language is used to define the planned architecture (VHDL). The neural network was trained using the MATLAB program, and the hardware implementations were created and tested on an Altera DE2-70 FPGA [9]. also showed that using the standard principal component analysis approach, some experiments with ear and face recognition revealed that the recognition performance is essentially identical whether using ear or face images, and that combining the two for multimodal recognition results in a statistically significant performance improvement. PCA-based face recognition is described in [10], with different testing criteria. The recognition rates vary depending on the number of training and testing sets used size of the image and even presence of noise in the face images. Its inherent advantage is that it preserves the spatial information of image samples while also being resilient to outliers.

An automatic extraction of a collection of geometrical attributes from a facial image, including nose width and length, mouth position, and chin shape was demonstrated in [11]. From a 35-dimensional vector, 35 characteristics were retrieved. A Bayes classifier was then used to perform the recognition. While a single layer feed forward ANN technique along with PCA to determine the optimal learning rate for reducing training time was [12] employed. They demonstrated the superiority of variable learning rate over constant learning rate. They put the system through its paces in terms of recognition rate and training time. Also a face recognition system with incremental learning ability that has one-pass incremental learning and automatic generation of training data was presented in [13]. They adopted Resource Allocating Network with Long-Term Memory (RANLTM) as a classifier of face images. Also [14] showed a hybrid face recognition method that combines holistic and feature analysis-based approach using a Markov random field (MRF) model. The MRF model is utilized to express the relationship between the image patches and the patch IDs, and the face images are separated into small patches. Given a test image, the MRF model is first learnt from the training image patches. The belief propagation (BP) HM is then used to infer the most likely patch IDs. Finally, a voting system is used to decide the image's ID from the estimated patch IDs. A PCA-based facial recognition system with a variety of testing conditions was described in [15]. The recognition rates vary depending on the number of training and testing sets used size of the image and even presence of noise in the face images.

3. METHODS

The study was based on a system that collects a user's face appearance in order to match it with another face. As illustrated in Fig. 1, the system consists of four primary components: face detection, eye region detection/alignment, feature extraction, and matching, with localization and normalization (face detection and alignment) serving as processing steps preceding face recognition (facial feature extraction and matching).

Fig.1. Processes involve in the system

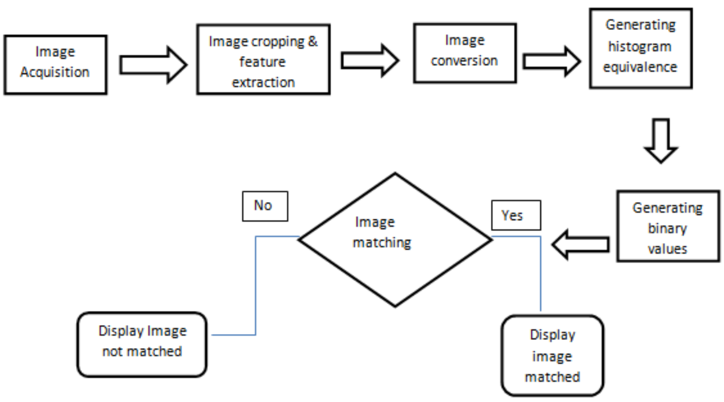


Fig. 2. Block Diagram of the system

Viola Jones algorithm was used to implement the face detection stage, It is a preferred algorithm for frontal face detection due to its higher accuracy and better adaptability to real time situations. MATLAB software was used for the viola jones algorithm. Image capture and preprocessing were the first steps in face detection. The image's histogram equivalence was created, in which the histogram values were converted to binary, which was then read in the HDL program. Lastly Hamming Distance was chosen as a matching metric since it calculated the number of bits that differed between two templates. When calculating the hamming distance between two templates, one is shifted left and right bitwise, and a series of hamming distance values are calculated from the shifts. To account for rotational inconsistencies, a threshold limit was specified, where the picture pixel difference was calculated and the system displayed image not matched if the test image fell within this value, otherwise image matched.

3.1 Implementing on FPGA Chip

VHDL was used to implement the system on FPGA. For the recognition stage, the binary data values from the histogram were employed. Network training was done in MATLAB for ease of implementation on FPGA. The face recognition stage was implemented using an MLP neural network with the goal of improving recognition accuracy. As a result, the required hardware will be less sophisticated, and the face detection system will be faster. It is important to transfer images in a standard format into a file that the VHDL file read procedure can understand in order to process real image data in VHDL simulations.

The hardware system was fully implemented on an FPGA, VHDL Top level consists of small components. All these components were designed in VHDL by using Xilinx ISE (13.4) design suite.VHDL statements are essentially parallel, not sequential, therefore building and designing the full algorithm using FPGA will help in speedup the execution time of the processes and this will lead in speeding the overall system execution of the face recognition. When the simulation was done successfully, the program will output or display a result of image matched or image not matched. The program was then prepared for installation on the Spartan-3AN starting kit shown in Fig. 3. The kit includes many input and output pins that can be configured as required.

Fig. 3. FPGA board (Spartan-3AN starter kit)

A conventional high-density (HD-DB15) VGA female connector display port was used to connect the FPGA board to the Video Graphic Adapter (VGA) monitor. The architecture was created with the goal of displaying the findings on a VGA monitor and creating a self-contained FPGA device that could be monitored. RED, Green, Blue, vertical synchronous (vsync), and horizontal synchronous (hsync) signals were used to link the board to the VGA (hsync). Each of the signals, Red, Blue, and Green, is made up of four bits. The color gradations displayed on the screen will be controlled by these signals. The 4-bits for each signal will give 4–bits resolution for each color, thus creating 12-bit colors, or 4,096 possible colors since each color has 16 possible value and this will lead to 16 possible colors.

4. RESULTS AND DISCUSSION

The simulation programs for the face detection, training, and testing stages for ANN models were written in MATLAB software. Starting with reading an image and detecting the face from the image, the Viola Jones method was utilized to achieve each outcome step. As illustrated in the Fig. 4 (abc) below, a boundary box was constructed to show the faces in each image.

The next step was to detect the eye portion; rather than considering the entire face, specific areas of the face were excised in this study, which is known as hemi-facial extraction. A face detector was developed that detects the eye region of the face by drawing a boundary box around the eye section of the faces. Fig. 5 illustrates the picture of eye region detected from the sample images.

The image was transformed to black and white, or gray-scale, to simplify the complexity of the operation utilizing a colored image. Each image's binary and histogram equivalence was calculated; as seen, there is a significant variation in both the histogram and binary equivalence between these images, as well as varied intensities in the plots. In both binary and histogram graphs, the eye component of different sample images yields varying intensities.

Fig. 4a. face detection of image A

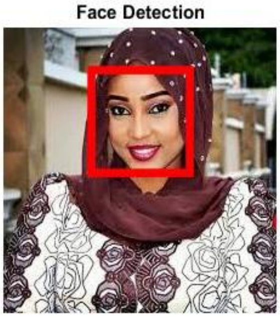


Fig. 4b face detection of image B

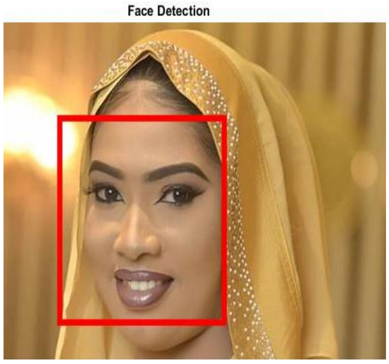


Fig. 4c face detection of image C

Fig. 5a Eye detection image A

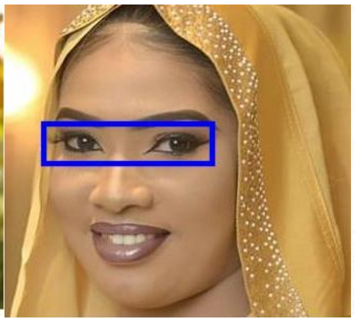
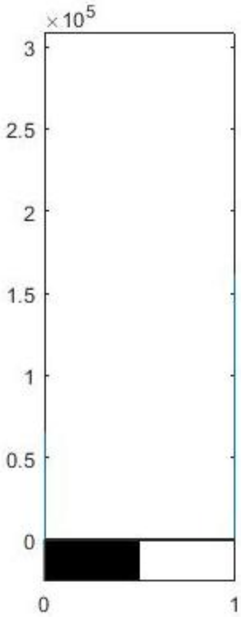
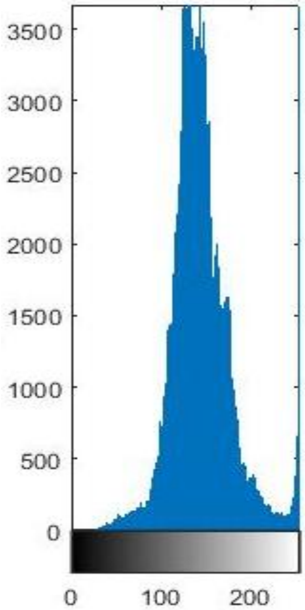


Fig. 5b Eye detection image B

Fig. 5c Eye detection image C



(a)



(b)

Fig. 6a and b. Binary equivalence ofsample image Cand Histogram equivalence of image C

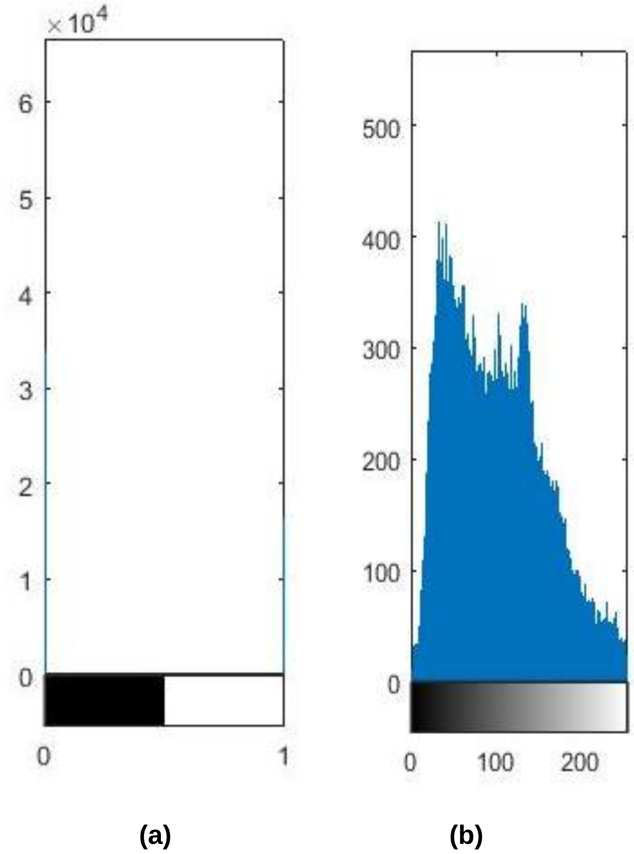


Fig. 7a and b. Binary equivalence of sample image A and Histogram equivalence of sample image A

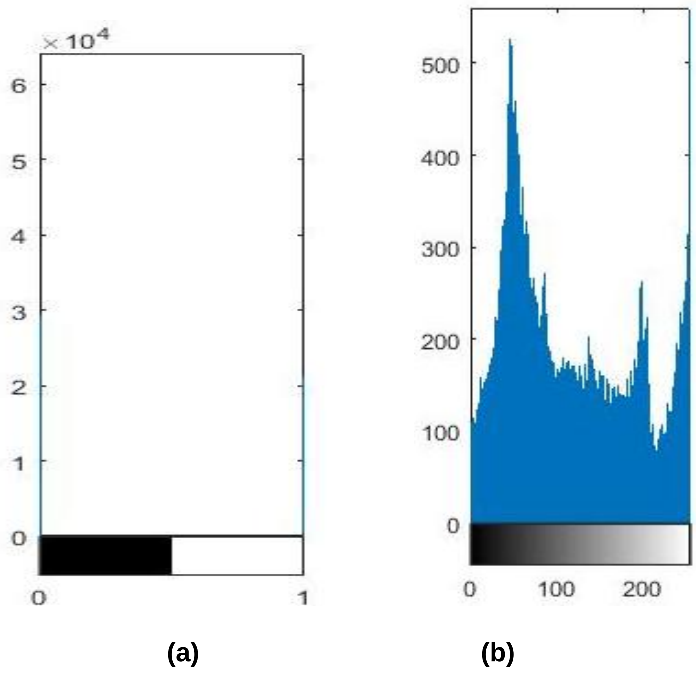


Fig. 8a and b. Binary equivalence of sample image B and Histogram equivalence of sample image

Table 1. Device Utilization of FPGA

Logic Utilization	Used Number	Available Number	Used Ratio %
Number of DSO48E1s	2	3360	0
Number of Slices Register	2057	142400	0
Number of fully used LUT-FF	2050	111712	1
Number of Slice LUTs	111705	712000	15

Table 2. Recognition Results

Sample images	Recognition results
Image A & Image B	Image not matched
Image A & Image A	Image matched
Image A & Image C	Image not matched
Image B & Image B	Image matched
Image B & Image C	Image not matched
Image C & Image C	Image matched

In the final stage, the binary values of the data were created; these two binary image files were compared using the XOR operation. A comparison with a software solution was done using a computer with an Intel Quad-core i7-2600 CPU to gain more insight into the performance of the FPGA-based implementation. Matlab was used to develop the software, and VHDL was used to program the FPGA as mentioned above. VHDL statements are essentially parallel rather than sequential. As a result, the programmer can use VHDL to create parallel programs. The AND and XOR functions, as well as the Hamming distance algorithm's summation procedure, are paralleled by the architecture design in the FPGA. If an image sample is 48x240 pixels, 11,520 matching elements are required. The FPGA architecture design performs 11,520 bits of XOR process between sample A and sample B or C. In addition, performing 23,040 bits of ANDing, parallel summation between bits and calculating the ratio of the number of differences between the template, only in one single clock cycle. These highly reduce the execution time of the system. Table 1.0 shows the device utilization in the FPGA.

However, from a power consumption point of view GPUs spend tens of times more power than FPGAs in terms of power usage. This makes FPGAs a more appealing solution, particularly in battery-powered devices. The simulation was done successfully, and the program output or display a result of image matched or image not matched as seen in Table 1 below corresponding to the threshold limit specified.

5. CONCLUSION

FPGA based facial recognition system was presented in this work to recognize facial images with a focus on the eye area of the face. Matlab was used to develop the software, and VHDL was used to program the FPGA (Spartan-3AN starter kit) and to compare in order to get further insight in the performance of the FPGA based implementation using an Intel Quad-core i7-2600 CPU computer. The algorithm was able to distinguish between two images of people based on their eye image, as well as detect minor expressional changes in the test image. Designing the full algorithm using FPGA help in speeding up the execution time of the processes by reducing the number of clock cycles needed in the execution of the program, which leads to the speeding of the overall system,it also gives the opportunity to build the system to work in real time with low cost due to its flexibility. In the future, it is recommended to use the iris of the eye to perform the recognition.

DISCLAIMER

The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge.

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COMPETING INTERESTS

Authors have declared that no competing interests exist.

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