



AC Analysis of Differential Active Balun Topology

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Author's contribution

The author designed, analyzed, interpreted and prepared the manuscript.

Article Information

DOI: 10.9734/JERR/2020/v10i417043

Editor(s):

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Complete Peer review History: <http://www.sdiarticle4.com/review-history/53990>

Received 16 December 2019
Accepted 24 February 2020
Published 27 February 2020

Original Research Article

ABSTRACT

The current manuscript aimed to study a differential active balun circuit in terms of the small-signal analysis, implemented in a standard 90-nm complementary metal-oxide semiconductor (CMOS) technology. Small-signal or alternating current (AC) response or frequency response of the active balun determines the maximum frequency of operation and the effective bandwidth of the circuit. With the analysis, the active balun circuit could be modeled and designed to achieve gain or attenuation at the desired frequency of operation. Design tradeoffs are inevitable and are carefully considered in the analysis and design. Eventually, the differential active balun design achieved a gain difference better than 1 dB and a phase difference of $180^\circ \pm 10^\circ$ or better at the frequency of operation of 5.8 GHz, comparable to previous designs and researches.

Keywords: AC analysis; differential active balun; small-signal analysis; transconductance; voltage gain; CMOS.

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1. INTRODUCTION

Radio frequency (RF) front-end blocks or circuits are often designed as differential in topology. Fully-differential approach is usually preferred in integrated circuit (IC) design due to its many advantages [1-3]. In order to supply input signal to differential circuits, a building block capable of supplying balanced differential signals is needed without sacrificing the performance of the overall system in terms of gain, noise fig., and linearity. An active balun (balanced-unbalanced) can perform the required tasks.

Active baluns are preferred over their passive counterparts because they can operate at higher frequencies, occupy less chip area, and can produce gain. One active balun topology is the differential active balun [3,4] shown in Fig. 1. It consists of 3 transistors: M1 and M2 as the differential outputs, and M3 for the tail current. The circuit in focus in this paper is designed in a standard 90-nm CMOS process. The input signal fed in one of the differential pair transistors will ideally split equally between the transistor pair, resulting to same amplitude and 180° phase difference [4].

2. CIRCUIT ANALYSIS AND DISCUSSION

To check if the designed active balun circuit would normally produce gain or attenuation at the desired frequency of operation, it is necessary to analyze and study the alternating AC response or frequency response or the small-signal response of the circuit. Moreover, through the small-signal analysis, the frequency range of operation of the circuit and the effective bandwidth could be determined [5-8].

The small-signal equivalent circuit of the differential active balun topology in Fig. 2 shows the tail resistor (R_{tail}) as the output resistance of transistor M3. Intrinsic capacitances are identified in the model, with output load capacitances (C1 and C2). The active balun circuit is driven by a finite source resistance (R_s).

A simplified small-signal model of the differential active balun circuit is shown in Fig. 3. This time, the effects of the capacitances are neglected. Noted here is the input of the active balun connected to the gate of M1, thus input resistance (R_{in}) $\rightarrow \infty$. R_s is also neglected in the model.

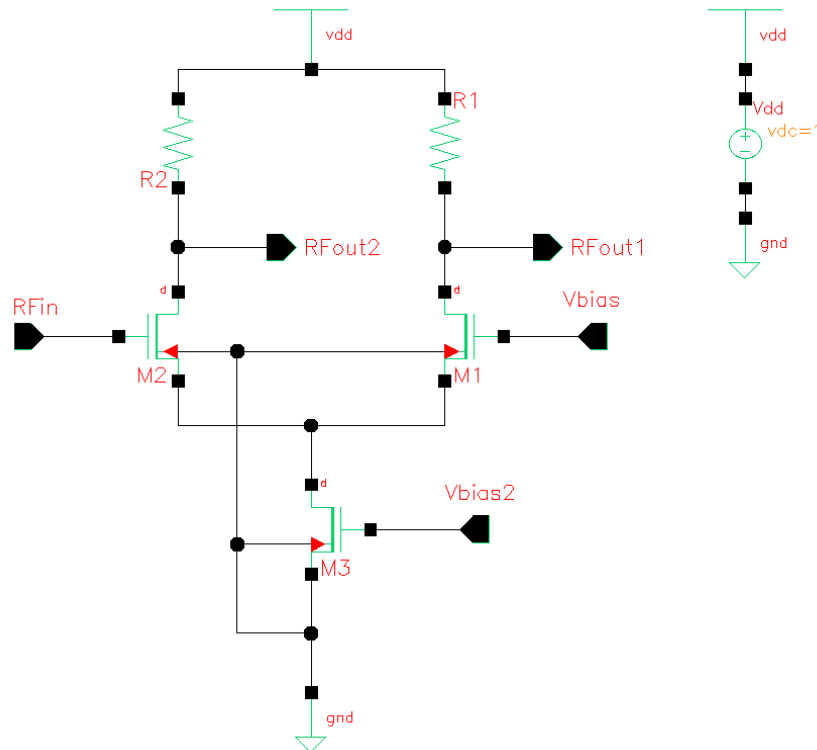


Fig. 1. Differential active balun circuit topology

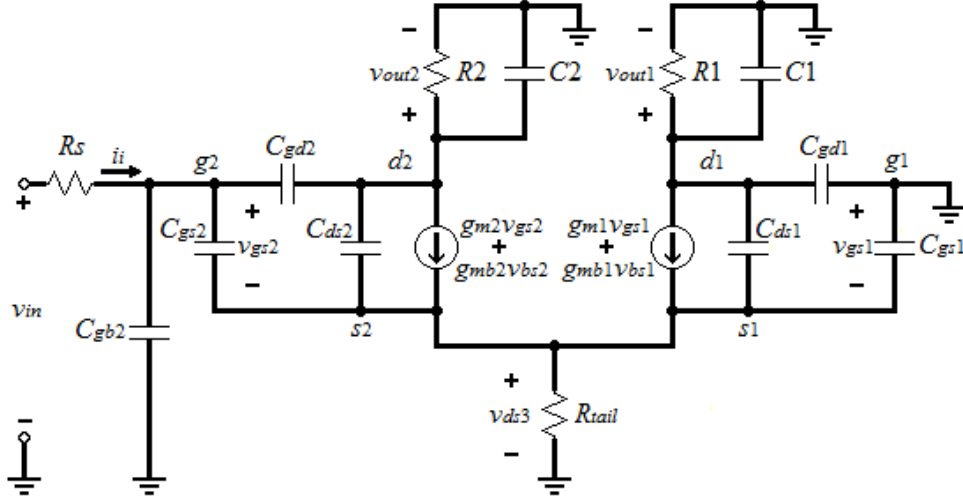


Fig. 2. Differential active balun topology small-signal model

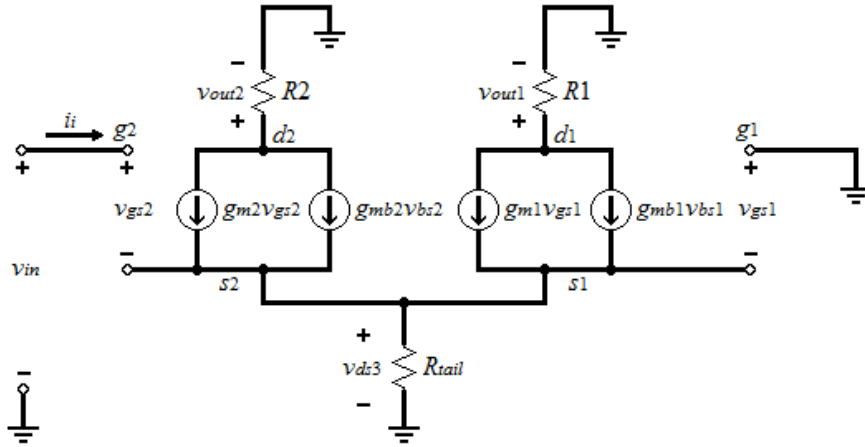


Fig. 3. Differential active balun topology low frequency small-signal model

Resistor R_{tail} effectively represents M3 since the tail current equates to zero with the gate voltage (v_{g3}) and source voltage (v_{s3}) both connected to ground. Applying Kirchhoff's Circuit Law (or simply KCL) on the drain node of M3 or source nodes of M1 and M2, results to the expressions below.

$$g_{m2}v_{gs2} + g_{mb2}v_{bs2} + g_{m1}v_{gs1} + g_{mb1}v_{bs1} = \frac{v_{ds3}}{R_{tail}} \quad (1)$$

$$v_{ds3} = \frac{g_{m2} \cdot v_{in}}{G_{m1} + G_{m2} + \frac{1}{R_{tail}}} \quad (2)$$

$$\text{with } G_{m1} = g_{m1} + g_{mb1} \text{ and } G_{m2} = g_{m2} + g_{mb2} \quad (3)$$

A relationship between the input small signal (v_{in}) and the voltage drop (v_{ds3}) is now expressed in (2). This equation is essential for computing the voltage gains, A_{v1} and A_{v2} .

$$A_{v1} = \frac{v_{out1}}{v_{in}} = \frac{g_{m2} \cdot G_{m1}R1}{G_{m1} + G_{m2} + \frac{1}{R_{tail}}} \quad (4)$$

$$A_{v2} = \frac{v_{out2}}{v_{in}} = - \frac{(g_{m2} \cdot G_{m1}R2) + (g_{m2} \cdot \frac{R2}{R_{tail}})}{G_{m1} + G_{m2} + \frac{1}{R_{tail}}} \quad (5)$$

If the differential active balun topology is assumed to be balanced, with transconductance

$G_{m1} = G_{m2}$, and with ideal tail current source such that $R_{tail} \rightarrow \infty$, voltage gains (A_{v1} and A_{v2}) could be simplified.

$$A_{v1} = \frac{v_{out1}}{v_{in}} = \frac{g_{m2} \cdot G_{m1} R1}{G_{m1} + G_{m1}} = \frac{g_{m2} R1}{2} \quad (6)$$

$$A_{v2} = \frac{v_{out2}}{v_{in}} = -\frac{g_{m2} \cdot G_{m1} R2 + 0}{G_{m1} + G_{m1}} = -\frac{g_{m2} R2}{2} \quad (7)$$

Voltage gains would be equal if load resistors $R1 = R2$. Note that this is a characteristic of a balanced differential amplifier circuit.

$$|A_{v1}| = |A_{v2}| = \frac{g_{m2} R1}{2} = \frac{g_{m2} R2}{2} \quad (8)$$

Due to non-ideality, the output impedance of M3 is not high enough as required resulting to unequal signals in the two output branches [4,7,9,10]. One way to address the imbalance is to adjust the value of load resistors ($R1$ and $R2$). Equations in (6-7) would be the basis for the two voltage gains, respectively. These two equations would result to the relationship of the load resistors with the transconductances and R_{tail} .

$$|A_{v1}| = |A_{v2}| = \frac{g_{m2} \cdot G_{m1} R1}{G_{m1} + G_{m2} + \frac{1}{R_{tail}}} = \frac{(g_{m2} \cdot G_{m1} R2) + \left(g_{m2} \cdot \frac{R2}{R_{tail}}\right)}{G_{m1} + G_{m2} + \frac{1}{R_{tail}}} \quad (9)$$

$$G_{m1} R1 = \left(G_{m1} + \frac{1}{R_{tail}}\right) R2 \quad (10)$$

$$R1 = \left(1 + \frac{1}{G_{m1} R_{tail}}\right) R2 \quad (11)$$

$$R2 = \left(\frac{1}{1 + \frac{1}{G_{m1} R_{tail}}}\right) R1 \quad (12)$$

where

$$G_{m1} = g_{m1} + g_{mb1} \quad (13)$$

The expressions for load resistors ($R1$ and $R2$) indicate the factors of output resistance (R_{tail}) and transconductance (G_{m1}). This confirms the imbalance relationship of the differential active balun circuit, given the non-ideal current source

that is transistor M3. Output voltages (v_{out1} and v_{out2}) depend on the corresponding transconductances of the branch transistors (M1 and M2). High transconductance would help minimize the imbalance, but in turn would increase the power consumption. A better way to mitigate the problem is to set the transistor efficiency ($g_{mover1d}$) high enough. Increasing load resistors ($R1$ and $R2$) would increase the voltage gains (A_{v1} and A_{v2}), respectively. Nevertheless, with the power consumption requirement, there is a limit in the effectiveness of increasing $R1$ and $R2$. With transistor dimensions set identical for the branch transistors (M1 and M2), fine-tuning could be made at the output loads ($R1$ and $R2$). Design tradeoffs are unavoidable; hence, they are carefully considered in the design of the differential active balun circuit.

3. CONCLUSION AND RECOMMENDATIONS

A differential active balun topology is designed and implemented in a standard 90-nm CMOS process, and critically designed to satisfy the RF requirement particularly the WIMAX standards [11]. Discussions on the AC analysis or the small-signal analysis is presented. It is essentially important to study and analyze the AC response or frequency response or small-signal response of the differential active balun to determine the frequency of operation, the desired gain or attenuation, and the effective bandwidth of the circuit [4,7,10]. For this active balun topology, the design achieved a gain difference better than 1 dB and a phase difference of $180^\circ \pm 10^\circ$ or better at the frequency of operation of 5.8 GHz. The values are comparable to previous designs and researches [12-14].

Future studies could include designing active balun with high gain. Although it will sacrifice the bandwidth, it can still be realized at lower frequencies for practical applications. One possible work would be to integrate the active balun functionality on the circuit design of a differential circuit like that of the double-balanced mixer or differential LNA.

DISCLAIMER

The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for

any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

ACKNOWLEDGEMENT

The author would like to extend appreciation to the Department of Science and Technology (DOST), DOST-PCASTRD, DOST-ERDT, and to the Microelectronics and Microprocessors Laboratory (Microlab) of the University of the Philippines esp. to Dr. MT De Leon and Dr. JR Hizon for the great technical support. The author would also like thank the STMicroelectronics Calamba New Product Development & Introduction (NPD-I) team and the Management Team for the extended support.

COMPETING INTERESTS

Authors has declared that no competing interests exist.

REFERENCES

1. Gray PR, Hurst PJ, Lewis SH, Meyer RJ. Analysis and design of analog integrated circuits. 4th Ed., New York: John Wiley & Sons, Inc.; 2001.
2. Jung K, Eisenstadt WR, Fox RM, Ogden AW, Yoon J. Broadband active balun using combined cascode-cascade configuration. *IEEE Transactions on Microwave Theory and Techniques*. 2008;56(8):1790-1796.
3. Gomez FR, De Leon MT, Roque CR. Active balun circuits for WiMAX receiver front-end. *TENCON 2010 – IEEE Region 10 Conference*. 2010;1156-1161.
4. Gomez FR, Hizon JR, De Leon MT. Differential active balun design for WiMAX applications. *Journal of Engineering Research and Reports*. 2019;4(4):1-8.
5. Razavi B. Design of analog CMOS integrated circuits. New York: McGraw-Hill; 2001.
6. Bowick C. RF circuit design. 1st Ed., USA: Howard W. Sams & Co. Inc.; 1982.
7. Frederick Ray I. Gomez, Maria Theresa G. De Leon, John Richard E. Hizon. CMOS differential active balun circuit small-signal analysis. *International Journal of Advanced Engineering and Technology*. 2019;3(3).
8. Baker RJ. CMOS circuit design, layout, and simulation, 3rd Ed. New Jersey: IEEE Press, 2010, New Jersey: John Wiley & Sons, Inc.; 2010.
9. Gomez FRI, Hizon JRE, De Leon MTG. Design and simulation study of active balun circuits for WiMAX applications. *Asian Journal of Engineering and Technology* 2019;7(01). ISSN: 2321–2462.
10. Frederick Ray I. Gomez, Maria Theresa G. De Leon, John Richard E. Hizon. CMOS differential active balun circuit small-signal analysis. *International Journal of Advanced Engineering and Technology*. 2019;3(3).
11. IEEE standard 802.16e-2005. Part 16: Air interface for fixed and mobile broadband wireless access systems, Amendment 2: Physical and medium access control layers for combined fixed and mobile operation in licensed bands, and Corrigendum 1. IEEE Computer Society and IEEE Microwave Theory and Techniques Society; 2006.
12. Ma H, Fang SJ, Lin F, Nakamura H. Novel active differential phase splitters in RFIC for wireless applications. *IEEE Transactions on Microwave Theory and Techniques*. 1998;46:2597-2603.
13. Do MA, Lim WM, Ma JG, Yeo KS. Design of a phase splitter for 3rd ISM band. *IEEE Conference on Electron Devices and Solid-State Circuits*. 2003;237-240.
14. Zhang HB, Cai M, Wu H, Chen HL. A 2.5GHz BiCMOS low noise and high-gain differential LNA for WLAN receiver. *Asia Pacific Conference on Postgraduate Research in Microelectronics and Electronics*. 2009;33-36.

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