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DESIGN OF HIGH PERFORMANCE DOUBLE TAIL COMPARATOR

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Abstract

Comparator is an important building blocks used in analog-to-digital converters. Its function is to compare two analog inputs and delivers a logic value at the output. In this project an analysis on the delay of various dynamic comparators are presented. Based on the analysis a new dynamic comparator is designed for fast operations. Positive feedback mechanism is used to regenerate the analog input signal into full scale digital level. This design is a modification of conventional double-tail comparator. Addition of a few transistors to the conventional double-tail comparator results in remarkably reduced time delay. Kick-back noise of this comparator is also reduced. The large voltage variations in the internal nodes are coupled to the input nodes, which will disturb the input nodes-this is called kick-back noise. This is reduced by inserting switches before the input transistors of comparator. The performance of conventional comparator and proposed comparator circuits are evaluated based on Cadence 180nm CMOS process models.

Keywords:

Analog to Digital Converter (ADC), Double Tail Comparator, Kick Back Noise

1. INTRODUCTION

Comparison is one of the basic operations used in analog to digital comparator. In the conversion process, input signal is sampled first. This sampled signal is then applied to the comparators to find the digital equivalent of the input analog value. Comparators give a logical value, which determine whether one input is higher or lower than the other one. The selection of an ADC is defined by the requirements: if we need speed, then use a fast ADC, if we want precision, use an accurate ADC, or if we are constrained in space, use a compact ADC.

Comparators produce a logical value, which indicates whether one input is higher or lower than the other one [8]. Nowadays, the demand for high speed ADCs is increasing. Since, comparators are the basic building block used in ADCs we require comparators with high speed, less delay and less kick-back noise. Kick-back noise is one of the major problems affecting the comparator and it will affect the accuracy of the analog-to-digital converter. Many techniques are available to reduce this issue.

Usually, dynamic comparators are preferred in ADCs because these comparators have less delay and less power consumption [7]. Positive feedback mechanism is provided by back-to-back inverters which converts a smaller voltage difference to full scale-digital level output.

When supply voltage is small, design of high-speed comparator becomes complex. A voltage boosting method is presented in [5] and this method is apt for CMOS design containing transistors with threshold voltage comparable to the supply voltage. Here, during comparison phase supply voltage is locally boosted to higher levels. Time delay of the comparator is reduced by liming the voltage swing of first stage to $V_{dd}/2$ in [12]. Some extra circuits are inserted to the conventional dynamic comparator to enhance the performance in [4] and [6]. A double-tail latch type comparator, which has high input impedance and full swing output, is proposed in [2].

Performance of a comparator can also explain in terms of the accuracy it provides. Uncertainty in the transition region of output is mainly due to noise.

This paper is divided into six sections, first section is the introduction. Section 2 is the literature review of this topic. Section 3 gives a brief idea about conventional dynamic comparators. Proposed double-tail comparator is presented in section 4. Simulation results are given in section 5. Finally, conclusions are drawn in section 6.

2. DYNAMIC COMPARATORS

Comparison of inputs is done at distinct time points in the case of dynamic comparators. These comparators require a clock or triggered signal. Dynamic comparators uses positive feedback to enhance the gain and have to make decisions in a limited time slot and. The working of dynamic comparators is divided in to two stages: reset phase and comparison phase.

2.1 CONVENTIONAL DYNAMIC COMPARATOR

Conventional dynamic comparator is a simple comparator used in ADCs since it has high input impedance, rail-to-rail output swing and no static power consumption. The schematic diagram of the conventional dynamic comparator is shown in the Fig1. The operation of this comparator can be divided in to two phases: reset phase and comparison phase.

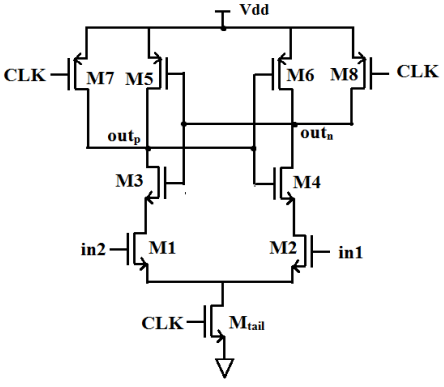

Fig.1. Schematic diagram of conventional dynamic comparator

During reset phase *CLK* is at 0V and during comparison phase, *CLK* is at V_{dd}. Inputs in_1 and in_2 are applied to the input transistors M_1 and M_2. In the reset phase, transistor M_{tail} is off. But, transistors M_5 and M_6 start conducting in reset phase and which pull up both the outputs out_p and out_n to V_{dd} to have a valid logic state during

reset. Then, as the time passes, the precharged outputs starts to discharge to ground depending on the inputs applied.

Assume $in_1 > in_2$, then out_n will discharge faster than out_p. Whenever, out_n falls below V_{dd}-V_{thn} before out_p, the corresponding pmos transistor M_5 start conducting and initiate regeneration. Finally, out_p will be pull back to V_{dd} and out_n discharges to ground. The reverse will be happen if $in_1 < in_2$.

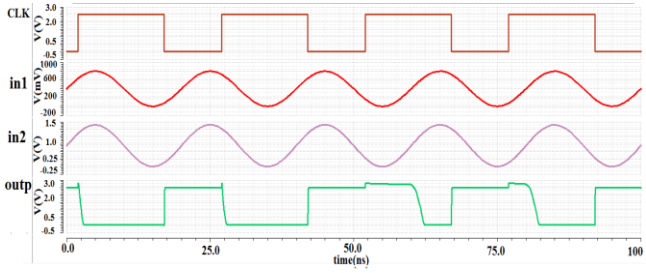

Fig.2. Simulation result of conventional dynamic comparator

Some problems exist in conventional comparator even though this structure has high input impedance and rail-to-rail output swing. First disadvantage is that, a sufficiently high supply voltage is needed for the proper working of the circuit due to several stacked transistors. There is only one current path via M_{tail} which contributes the current for both input stage and regeneration stage, which is the next problem. Because, each stage has its own current requirements like, input stage requires small current and regeneration stage requires large current to have fast regeneration. Transient simulation of design is shown in Fig.2.

2.2 CONVENTIONAL DOUBLE TAIL DYNAMIC COMPARATOR

The schematic diagram of the conventional double-tail is shown in Fig.3. This design has less stacking of transistors and therefore can be used at low supply voltages, which is the advantage of this topology.

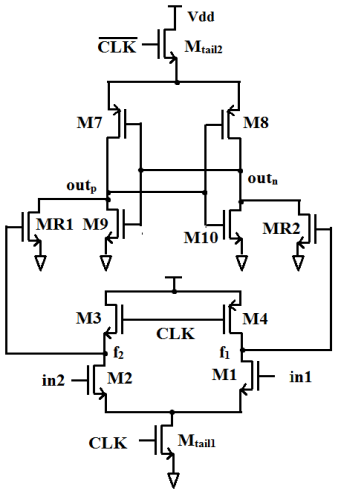

Fig.3. Schematic diagram of conventional double-tail comparator

In order to provide separate current path for regeneration path, one extra tail transistor is added to the circuit. Two intermediate transistors are indicated by MR_1 and MR_2 and intermediate points are denoted by f_1 and f_2. During reset phase, both tail transistors M_{tail1} and M_{tail2} are off. The intermediate points are pulled to V_{dd} by both M_3 and M_4 transistors. Then intermediate transistors turn on and which will cause both the outputs to discharge to ground. In the comparison phase, both tail transistors turn on and intermediate point voltage starts discharging depending upon the inputs applied. If $in_1 > in_2$, f_1 voltage discharge faster than f_2 voltage. So, out_p will be pull up to V_{dd} through M_7. Finally, out_p will be at logic high level. At the end of comparison stage both the intermediate point voltages discharges to ground, which is the main drawback of this circuit is that. So, these nodes have to be charged from ground to V_{dd} in the next reset phase, which may lead to increased power consumption.

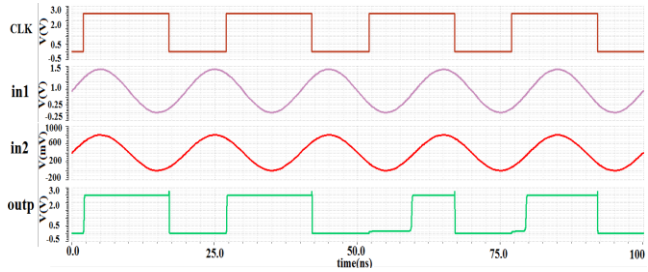

Fig.4. Simulation result of conventional double-tail comparator

By analyzing the conventional double-tail comparator, it can be concluded that delay of this circuit is inversely proportional to the difference in the input voltage ($\Delta V_{in1/in2}$). Difference in input voltage and difference in intermediate point voltage ($\Delta V_{f1/f2}$) are directly proportional. Hence increasing this difference would reduce the delay of the circuit. Transient simulation of the design is shown in Fig.4.

This double-tail comparator is much better than conventional one in terms of delay. But both the circuits are affected by kick-back noise problem. In latched comparators, the voltage variations on the output nodes may couple to the input nodes through parasitic capacitances. So, the input is disturbed, which may degrade the accuracy of the converter. This disturbance is called kick-back noise. Many techniques are available to reduce this noise in comparator circuits.

3. PROPOSED DOUBLE TAIL COMPARATOR

The Proposed double-tail comparator without noise reduction is demonstrated in Fig.5. The Proposed double-tail comparator with noise reduction technique is demonstrated in Fig.7. As explained in the previous section, it requires increasing intermediate point voltage ($\Delta V_{f1/f2}$) to reduce delay.

3.1 PROPOSED COMPARATOR WITHOUT NOISE REDUCTION

In order to increase the difference in intermediate point voltage, two control transistors MC_1 and MC_2 are added to the intermediate point in a cross-coupled manner [1].

Operation of the proposed comparator is as follows. During reset phase ($CLK = 0$), both tail transistors are off. The f_1 and f_2 voltages are pulled up to V_{dd} through M_3 and M_4. In the comparison phase ($CLK = V_{dd}$), intermediate point voltages start to discharge. Suppose $in_1 > in_2$, then f_1 discharge faster than f_2. As

f_1 continues discharging, the corresponding control transistor (MC_1) turns on, which will pull-up out_p back to V_{dd}.

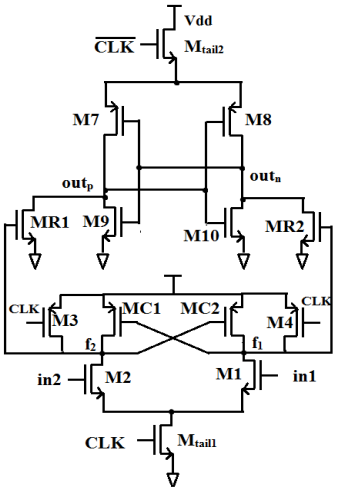

Fig.5. Schematic diagram of proposed comparator without noise reduction

This will cause the complete discharging of f_1 to ground. Finally out_p will be at V_{dd} after comparison. Advantage of this circuit is that during the reset stage, it is not needed to pull both f_1 and f_2 back to V_{dd} since, one of the points have already been pulled to V_{dd} in the previous comparison phase itself. Transient simulation of this design is shown in Fig.6.

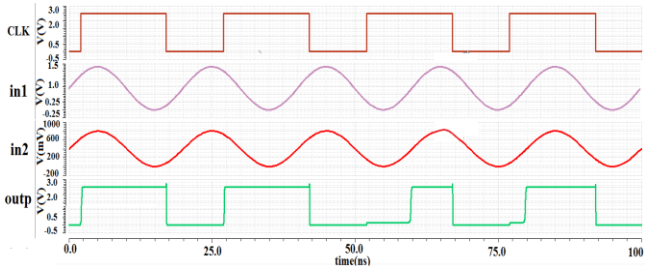

Fig.6. Simulation result of proposed comparator without noise reduction

3.2 PROPOSED COMPARATOR WITH NOISE REDUCTION

Kick-back noise is one of the major problems in comparators because; it may affect the precision of analog-to-digital converters. Many techniques are available to reduce this noise. Drains of the comparator are isolated from the output nodes using switches to eliminate the disturbances in [9]. But, disturbances arise during comparison phase also. Neutralization technique is introduced in [10] and [11] in which capacitors having equal magnitude as that of parasitic capacitance are added to the circuit. But, this technique also cannot achieve a significant noise reduction.

The Fig.7 shows the proposed comparator with kick-back reduction technique. This method can be used in any latched comparator [3]. Noise can be reduced by preventing any disturbances on the input nodes coupled from the output points. This is achieved by inserting switches before the input transistors of comparator.

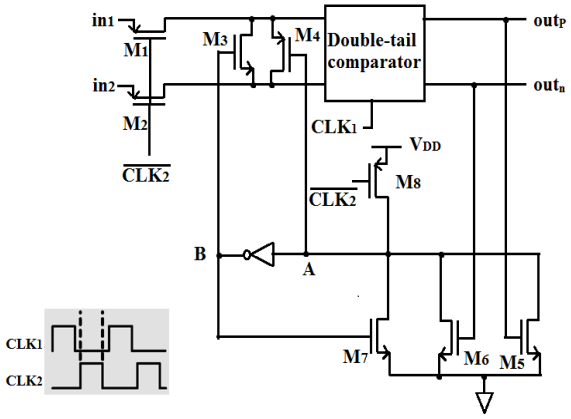

Fig.7. Schematic diagram of proposed comparator with noise reduction

In Fig.7, the box represents the proposed comparator circuit without noise reduction. Transistors M_1 and M_2 represents the control transistors. The M_3 and M_4 are the reset transistors. The CLK_1 is used to synchronize the operation of comparator and CLK_2 synchronizes operation of noise reduction circuit. When $CLK_1 = 0$ ($CLK_2 = V_{dd}$), comparator is in reset phase. Both input switches are on. Node A is pulled to V_{dd} through M_8 transistor and hence node B is at 0V. So, both reset transistors are off. Comparator reset both its outputs to logic low level. At the end of CLK_2, M_1 andM_2 turn off, hence preventing any disturbances from the output on the input points during regeneration.

During regeneration ($CLK_1 = V_{dd}$ and $CLK_2 = 0$), one of the two inputs will be pulled to high level, which will turn on M_5 or M_6 and hence pull down node A to ground. Finally both the reset transistors M_3 and M_4 turn on and reset the inputs. With this method, kick-back noise in the comparator circuit can be eliminated to a large extend.

4. SIMULATION RESULTS

In order to compare the proposed comparator with other conventional comparators, all the circuits have been simulated in 180nm CMOS technology with V_{dd} = 2.5V. The transient simulation of proposed circuit with noise reduction technique is shown in Fig.8.

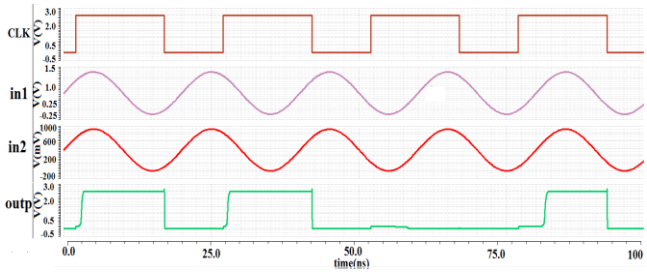

Fig.8. Simulation result of proposed comparator with noise reduction

The Table.1 shows the delay and kick-back noise of various circuit types like conventional comparator, conventional double-tail comparator, and proposed comparator without noise reduction technique and with noise reduction technique.

Table.1. Comparison of delay and noise of comparators

Circuit Type	Delay (in ps)	Kick-Back Noise (in mV)
Conventional comparator	285.46	404.5
Conventional double-tail comparator	105.32	301.7
Proposed double-tail comparator without noise reduction	75.51	299.3
Proposed double-tail comparator with noise reduction	80.27	95.3

It is clear from the table that the delay of conventional comparator was about 285.46ps. Delay is reduced to 105.32ps for conventional double-tail comparator. This is because there are two tail transistors, one of which provides enough current for the input section and the other transistor provides enough current for the regeneration section. The main advantage of this circuit is that it has reduced stacking effect. So, all the transistors will get enough current for the operations and delay is reduced.

In the proposed comparator the delay is about 75.51ps and 80.27ps. This is because of the two control transistors added. These will help in increasing the difference in intermediate voltage as time passes. Delay is inversely proportional to the difference in intermediate voltage and hence reduced the delay.

Kick-back noise of the conventional comparator was about 404.5mV. It is reduced by an amount of 300mV to 95mV. This reduction is achieved by adding two switches at the input, which will be opened during comparison phase so that feedback from output to the input can be reduced.

5. CONCLUSION

In this paper an analysis on the delay of dynamic comparators is presented. Conventional dynamic comparator and conventional dynamic comparator were analyzed initially. Then from the conclusions, a new double-tail comparator with less delay was proposed. Kick-back noise reduction technique is also included in this design. Simulation results in 180nm CMOS technology shows that this design considerably reduces the kick-back noise of the comparator. Other existing noise reduction techniques do not solve the problem significantly. On analysis using Cadence tool kit, the proposed circuit is able to reduce the delay by 200ns and kick-back noise by an amount of 300mV. As a future work, the offset of this comparator can be improved using some other techniques.

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